

# A LOW LOSS PTFE-BASED BOND PLY MATERIAL FOR MULTI-LAYER PCB APPLICATIONS

Growing needs are developing for pure package high performance, low loss laminate and prepreg materials for microwave telecommunications and high speed digital printed circuit board (PCB) applications. Polytetrafluoroethylene (PTFE), perhaps better known by the DuPont trade name, Teflon, has an over 30-year long history of meeting the needs in microwave frequency applications. PTFE-based materials reinforced with woven glass fabric and ceramic fillers offer the advantages of very low loss (<0.004 at 10 GHz), predictable dimensional stability and thermal reliability. Widespread adoption of PTFE-based laminates as an industry standard material has been slowed by the perception that PTFE-based solutions are expensive and must be processed differently. However, that perception is changing. Increased production volumes driven by the growth in the cellular telecommunications infrastructure and the development of lower cost PTFE-based laminates has driven the cost down such that the price/performance ratio is competitive to other material solutions

for high speed digital and hybrid microwave applications. The well known performance, improved processing techniques and reliability of PTFE-based substrates in high frequency applications provides the industry with a known solution that compares favorably to alternatives that include expensive glass styles, thermoplastic resin systems that do not flow or are low temperature, and elastomeric resin systems that do not bond well.

Drilling, routing, and plated through hole pretreatment and plating are no longer hurdles to be overcome for processing PTFE-based substrates. However, a recognized hurdle for building PTFE multi-layers has been a user-friendly bonding solution.

To address this need, a very low loss bonding ply comprised of a PTFE/woven fiberglass/ceramic/thermoset resin composite that can be processed at conventional PCB pressures and temperatures has been developed.

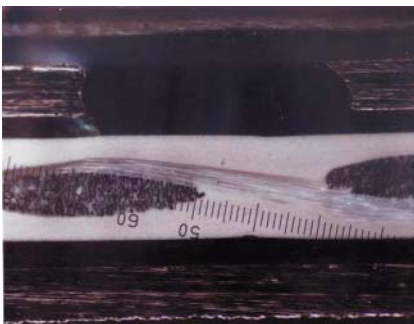
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# PRODUCT FEATURE

**TABLE I**  
**TP-32 PRELIMINARY DATA**

Property	Typical Value	Method
Glass transition (°C)	172.73	DSC
Pressed thickness (mil)	3.2 to 3.7**	
Dielectric constant (tba) at 10 GHz	3.29	IPC-TM 650 2.5.5.5
Dielectric loss at 10 GHz	0.004 to 0.005	IPC-TM 650 2.5.5.5
Moisture absorption (%)	0.014 to 0.240	IPC-TM 650 2.6.2.1
Peel strength (1.0 oz. ed) (lbs/linear inch)	5 to 6	IPC-TM 650 2.4.8
**Pressed thickness will vary depending on copper trace density and type of copper (0.5 to 2.0 oz.).		



▲ Fig. 1 A magnified cross-section showing the TacPreg material filling the internal circuitry.

This prepreg, when combined with the corresponding low loss laminate, provides the design engineer with a pure package approach for realizing exceptional electrical performance. The overall composite contains from 10 to 20 percent of a flowing thermosetting resin. The result is a composite that is sufficient to deliver a loss at 10 GHz of less than 0.005, peel strengths from 5 to 6 lbs, (sufficiently good to do foil laminations), good dimensional stability that enable the production of 20 to 40 layer count multi-layer circuits, gap filling of 1.0 oz. circuitry and drill performance exceeding standard PTFE boards. Because the composite is a hybrid of PTFE and a thermosetting resin, the composite has a rigidity similar to epoxy. The woven fiberglass reinforced composite enables the production of very high layer count PCBs with good layer-to-layer registration

because the processing at epoxy processing temperatures causes very little movement in the predominantly PTFE-based composite.

TacPreg is a patent pending technology that defines the composite mixing of thermoset resin with PTFE/woven fiberglass. The first TacPreg product is TP-32 with a di-

electric constant of 3.20 and loss tangent 0.005. **Table 1** outlines the TP-32 materials' preliminary specifications.

A 20-layer 0.190" thick 18" × 24" test vehicle was chosen to evaluate the material's process capability, electrical performance and thermal reliability. Surface foil lamination, various line widths down to 0.006" with 1 oz. copper and dielectric spacing of 0.008" using RF-35-008-C1/C1 laminate and TP-32-003 TacPreg bonding ply were chosen for the construction materials. The RF-35P laminate materials are available down to 0.002" thickness.

A series of prototype PCBs were successfully built and the information gathered from the boards continues to be evaluated. Additional tests continue to progress toward the development of more detailed processing window parameters. What follows is a basic overview of the results of these efforts. Specific detailed recommendations are available through the company for qualified project work.

## MATERIAL EVALUATION

The RF-35P laminate cores were processed using standard print and etch techniques. Standard copper adhesion promotion treatment was applied for bond enhancement. The layers were tested through standard automated optical inspection equipment. For this test vehicle, there

were no compensation factors used to evaluate the dimensional stability of the cores. It is anticipated that some compensation factors will need to be developed at the fabricator level for the different core thickness. **Figure 1** shows a magnification of the TacPreg filling of internal circuitry.

The boards were constructed with four plies of the TP-32 TacPreg between each core and to the surface with copper foil. The boards were laminated with an 8°F/min heat rise to the hold temperature of 400°F using pressure of 400 psi. The hold time was two hours and the cool down rate 10°F/min. The boards showed good filling and adhesion. The surface copper foil had peel strength of 6 lbs/in.

The boards were drilled using common practices; standard industry available drills, entry materials, and feeds and speeds for thick multi-layer boards. Specific drills, entry and backup, and feed and speed recommendations are being developed for fabrication guidance. The boards were plasma etched to treat the hole wall for plating adhesion promotion. A plasma cycle commonly used for PTFE materials in combination with thermoset resin constructions yielded good copper plating coverage.

The use of RF-35P and TacPreg TP-32 in this complex 20 layer count, 0.190" thick signal integrity printed circuit board has demonstrated a viable new low loss material for achieving high performance microwave and digital integrated functionality. The low temperature standard processing conditions for these materials will make them widely available to the OEM through the general printed circuit board fabrication infrastructure. TacPreg TP-32 is currently being produced on a preproduction basis and is available in limited quantities. Visit Taconic at MTT-S booth no. 423.

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