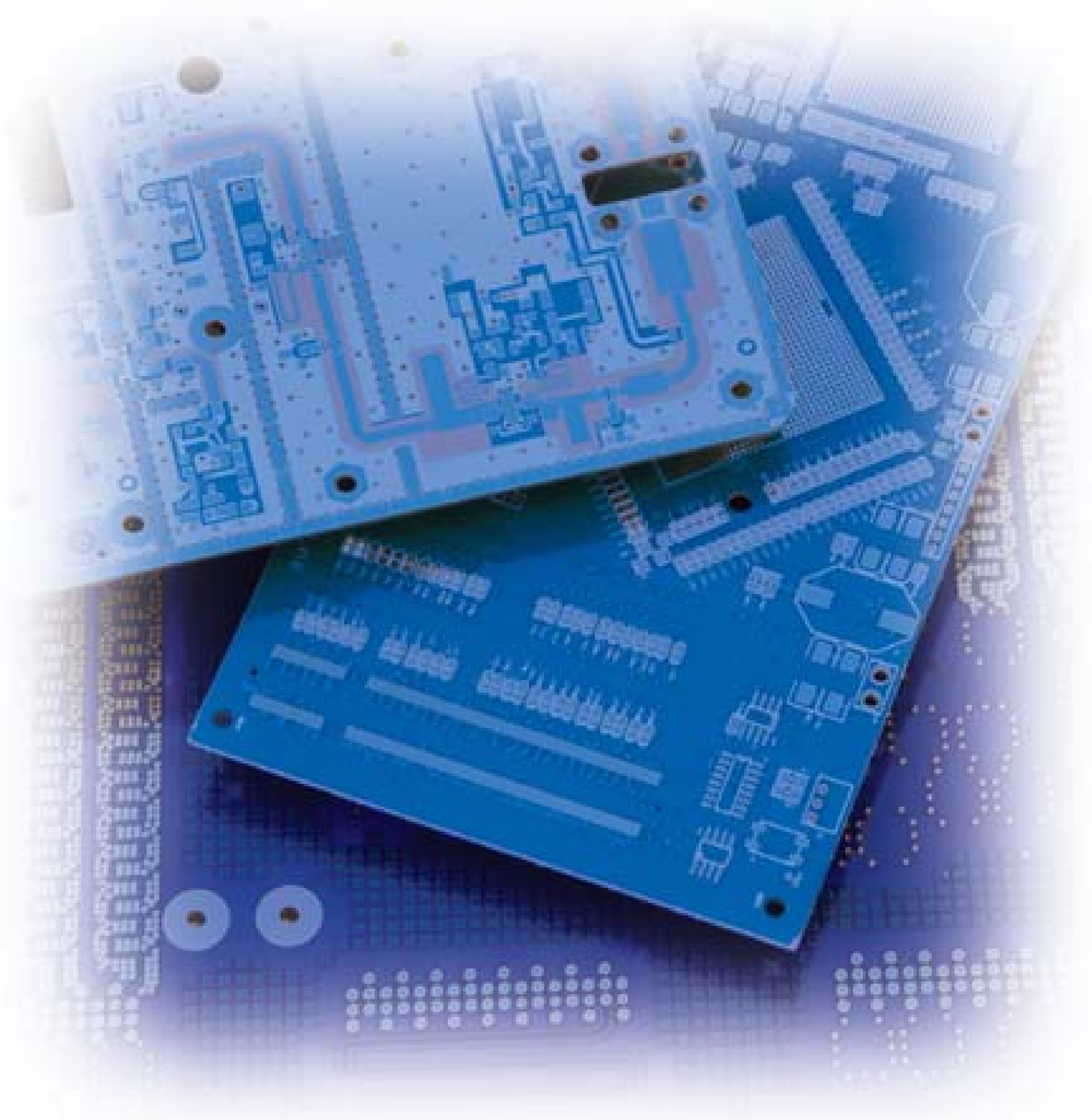
TacLam® TLG and TacPreg ®TPG Multilayer (TPG30, TPG32, TPG35) General Processing Guidelines



Petersburgh, NY – Tel: 800-833-1805 Fax: 518-658-3988
Europe – Tel: +353-44-95600 Fax: +353-44-44369
Asia – Tel: +82-31-704-1858 Fax: +82-31-704-1857
www.taconic-add.com
www.taconic.co.kr

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TacLam TLG and TacPreg TPG
General Processing Guidelines

Table of Contents

General Information

The TacLam® TLG laminate is part of the Taconic product offering designed specifically for the High Speed Digital market. Coupled with the TacPreg® TPG prepreg, TacLam® TLG enables the use of low electrical loss PTFE materials in high multilayer count boards with digital data rates exceeding 10 Gigabits per second. The thermoset properties of the bonding agent enable multiple laminations and thermal excursions during standard circuit board fabrication without delamination of the multilayer package.

TacLam® TLG-30, TLG-32 and TLG-35 utilize PTFE resin and ceramic for low electrical loss, woven fiberglass for dimensional stability, and a high performance thermoset resin as a bonding agent for the copper foil. The associated prepreg, TacPreg® TPG-30, TPG-32 and TPG-35, use the same materials with a partially cured thermoset resin to facilitate bonding of multiple inner layers of TacLam® TLG and/or foil cap layers. DESIGN NOTE: In order to achieve adequate filling around etched features, the number of TacPreg plies and ply thickness should be determined using the following guidelines in Table 1. These guidelines are based on high layer count multilayer designs with stacked traces which create high and low pressure areas during lamination. The recommendations are conservative and other designs may realize satisfactory results using fewer or thinner bond plies

Copper Weight	Tacpreg Product	Number of Plies
½ ounce	TPG-30-0045-35	1
½ ounce	TPG-30–0050-40	1
1 ounce	TPG-30-0045-35	2
1 ounce	TPG-30–0050-40	1
1 ounce plus plating	TPG-30–0050-40	2

Table 1 – TacPreg ply/thickness guidelines

For inner or outer layers requiring plating such as for blind or buried vias, two plies of TPG-30-0050-40 should be used as shown in the table above.

Processing TacLam® TLG can be readily accomplished using standard epoxy circuit board processing methods coupled with either plasma or sodium treatment of the PTFE hole walls. The following process recommendations are based on circuit boards produced at several facilities. It should be noted that each board shop may have different equipment and methods that will require modifications to these recommendations. Drill and routing parameters and artwork compensation data are very dependent on circuit board thickness and design and should be adjusted based on the experience of each facility. The treatment of hole walls prior to plating must be done using a plasma or sodium treatment system.

Material Properties					
	Dielectric Constant		Loss Tangent		Thickness Range
	10 GHz	1 MHz	10 GHz	1 MHz	
TLY	2.17 – 2.40		0.0009		0.0050” – 0.1870”
TLX	2.45 – 2.65		0.0019		0.0020” – 0.3750”
TLT		2.45 – 2.65		0.0006	0.0020” – 0.3750”
TLC	2.75-3.20		0.0030		0.0100” – 0.2500”
TLE	2.95-3.00		0.0028		0.0015” – 0.1250”
TSM-30	3.00		0.0015		0.0050” – 0.0600”
TPG-30	3.00		0.0038		0.0045” , 0.0050”
TLG-30	3.00		0.0026		0.0100” – 0.1200”
TPG-32	3.20		0.0050		0.0045” , 0.0050”
TLG-32	3.20		0.0030		0.0100” – 0.1200”
TPG-35	3.50		0.0050		0.0045”
TLG-35	3.50		0.0030		0.0100” – 0.1200”
RF-30	3.00		0.0014		0.0100” – 0.1200”
RF-35	3.50	3.50	0.0028	0.0018	0.0100” – 0.1200”
RF-35A2	3.50		0.0018		0.0050” – 0.0600”
RF-35P	3.50	3.50	0.0035	0.0025	0.0020” – 0.1250”
RF-41	4.10		0.0038		0.0600” – 0.1250”
RF-43	4.30		0.0033		0.0100” – 0.1250”
RF-45	4.50		0.0037		0.0200” – 0.1250”
RF-60A	6.15		0.0028		0.0100” – 0.1250”
Cer-10	10 (0.062 nominal)		0.0035		0.0040” – 0.1250”

Table 2 – Material properties

Handling of TacLam® TLG-30, TLG-32 and TLG-35 Laminates

PTFE is a thermoplastic material which is very stable electrically and chemically when compared with common thermosetting resins such as epoxy, polyphenyleneoxide, polyimide and cyanate ester. Part of what gives PTFE its superior performance over frequency and temperature also makes the pure resin relatively soft and dimensionally unstable. It is for this reason that all Taconic laminates are reinforced with glass fabric. The glass fabric reinforcement of the substrate greatly increases stability in the X and Y axis over non-woven or unreinforced PTFE products. While the glass fabric provides very good dimensional stability and increased stiffness, the relative softness of the PTFE resin requires that the following process and handling precautions should be taken to prevent damage or deformation of the laminate during fabrication.

- **Do not mechanically scrub the material**

As with thin core or flexible substrates, mechanically scrubbing will stretch and deform the material. The pinch rollers used to move the panel during scrubbing can also cause dents as particle or brush material are pressed into the surface of the laminate. Chemical cleaning is preferred. Eliminating mechanical cleaning and unnecessary handling will improve the dimensional accuracy of subsequent processes by preventing mechanical distortion of the laminate.

- **Do not pick up a panel horizontally by one end or edge**

By allowing the material to flop over you may stretch the copper and substrate. Lift the panel by two parallel edges; preferably the two closest dimensionally.

- **Prevent contaminant deposits on the material or copper**

The use of clean protective gloves and slip sheets will prevent contamination and staining. You will not need to remove oils, grease or fingerprints if you don't deposit them.

- **Do not stack panels directly on top of each other**

Particles or debris on the surface of the panel can become imprinted into the copper and substrate of adjacent panels. The preferred method of storage is to rack the panels vertically. If panels must be stacked use clean, soft, slip sheet material between each panel and keep stack height to a minimum.

Inner Layer Preparation

Multilayer applications require that two or more laminates be bonded together to form a single circuit board. There are two important considerations when processing the circuit board. The first is registration of the features from one layer to another. The second is the condition of the bond surface prior to lamination.

Registration: Layer to layer registration is often a critical requirement of the finished circuit board and misregistration can cause a variety of issues such as open circuits and poor coupler performance. Therefore, it is important that the material be acclimated to the processing environment and the correct artwork compensation used. Acclimation to the processing environment is simply making sure that the laminate is at ambient temperature prior to processing. It is recommended that if the laminate has seen extreme temperatures during shipment or storage, it should be placed in ambient conditions for 24 hours prior to processing.
All laminates experience movement after the copper foil has been etched. Various factors such as laminate thickness, glass style, construction, copper foil thickness, and circuit design all contribute to the characteristic known as dimensional stability. The dimensional change data for TacLam® laminates is listed below in Table 3. The data is reference only and, again, is dependent on the factors listed above. Most printed circuit board shops determine artwork compensation data by running samples or estimating based on previous experience.

Material Designation	Dimensional Change in Parts Per Million (PPM)
TLC	200 – 400
TLE	220 – 400
TLT	400 – 600
TLX	400 – 600
TLY	400 - 800
RF-35, 35P	200 – 400
RF60	400 – 600
Cer-10	400 – 600
TacLam® TLG	**200 – 400**

Table 3 – Typical dimensional change

Lamination

TacLam® TLG laminate is used in conjunction with TacPreg® TPG prepreg to produce multilayer boards for the digital market. TacLam® TLG laminate and TacPreg® TPG prepreg, when used in a symmetrical board design, will result in optimum electrical and mechanical performance. Because of the thermoset properties of the bonding agent, multiple bonding cycles can be achieved without worry of delamination. In addition, the recommended press temperature of 392°F [200°C] is within reach of most board shops. The TLG and TPG series of materials are highly ceramic filled like the TSM series of pure ptfe laminates. TSM is a ptfe-fiberglass-ceramic laminate like TPG/TLG but lacking a thermoset resin. However, TSM, when used as a laminate core, enables very low circuitry when combined with TPG30.

Taconic recommends the following press cycle:

- Vacuum Lamination Recommended
- Heat rise 3°F - 10°F / minute [1.5°C – 5.5°C] to 374°F [190°C] *
    - Flow window is 130°F [80°C] – 302°F [150°C]
- Maintain pressure at 73 psi [5 bar] until package reaches 100°F [37°C] then apply full pressure of 450 psi [31 bar]
- Hold (cure) for 1 hour
- Cool package under full pressure at < 6°F [3°C] / minute

*For high layer count boards, best flow and fill has been seen at low heat-up rates. For low layer count mulilayers, a low heat-up rate is less critical.

The prepreg cure is not very advanced. For best gap filling it is desirable to achieve the maximum amount of flow prior to the advancement of the resin. The earliest application of pressure will help, certainly below the melt of the epoxy (140°F [60°C]), coupled with a 3°F - 10°F [1.5°C -5.5°C] rate of rise. A cold start of the press is desirable. A hot start of the press will advance the cure of the resin before the best flow is achieved and the optimal amount of flow will not be achieved.

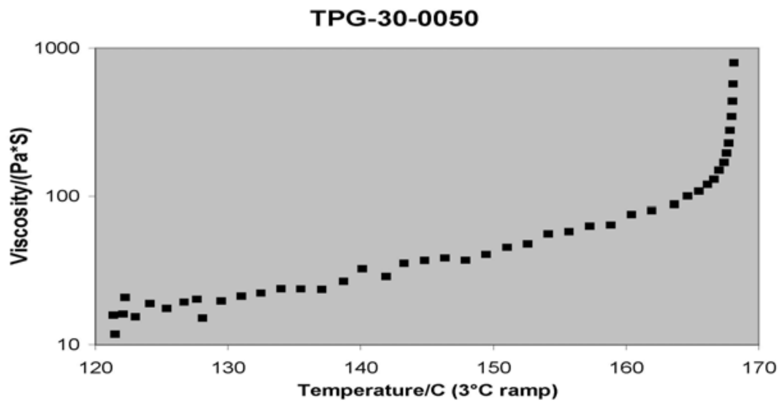

Figure 1 – TPG Viscosity

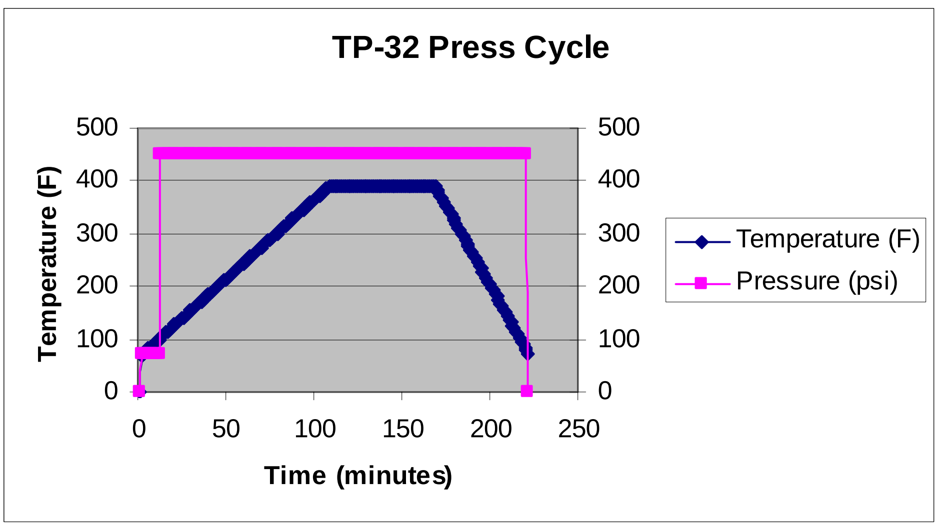

Figure 2 – TacPreg Press Cycle

Foil Lamination

For successful foil lamination with TPG the outer layer foil should have sufficient tooth structure to yield acceptable adhesion. If delamination occurs during foil lamination, the adhesion of a good section should be checked. If the adhesion is poor, a copper foil should be chosen with sufficient dendritic structure (TWS foil from Circuit Foils). If the adhesion is good the delamination likely is the result of thermal stresses. Cooling should never be done by transferring the laminates from a hot press to a cold press.

Cooling should be conducted in the multilayer lamination press at the slowest rate possible. Pacopadding will help stress relief, the thicker the better. Stress relief can also be accomplished by inserted a layer of flowing prepreg between the copper foil and the padding. The prepreg should be separated by some type of release film such that no contamination of the multilayer occurs. The construction should be press plate, release film, prepreg, release film, and then multilayer foil lamination. The prepreg will flow and offset thermal stresses. The prepreg can be FR4 or acrylic based polyimide prepreg. The goal is that the thermoset flow and offset thermal stresses. The release layer could be PTFE film, PVDF film, silicone coated paper etc.

Drilling for Double Sided TLG Laminate

Caution: for drilling thick multilayers please see the section on drilling thick multilayers.

It might be desirable to separately drill PTFE/ceramic or PTFE innerlayers during the manufacture of a multilayer using sequential lamination. If PTFE double sided boards are to be drilled separately, the drill parameters for a double side laminate core is not as critical as a thick multilayer. Because of the heavy silica loading and extreme fine glass style, double sided TLG offers a wide process window.

Good hole quality can be achieved using Taconic recommended drill parameters. Standard 130° point geometry, 32° - 35° helix angle PCB carbide drills work well with all Taconic PTFE-based laminates. Using maximum vacuum on the drill machine, quality drill bits, and optimizing the speeds and feeds is recommended if the birdnesting affects the plated through hole quality. The primary objective in drilling is to keep heat build up on the drill to a minimum. Hole quality is affected by drill sharpness; therefore Taconic recommends using new, brand name drills for the best hole quality.

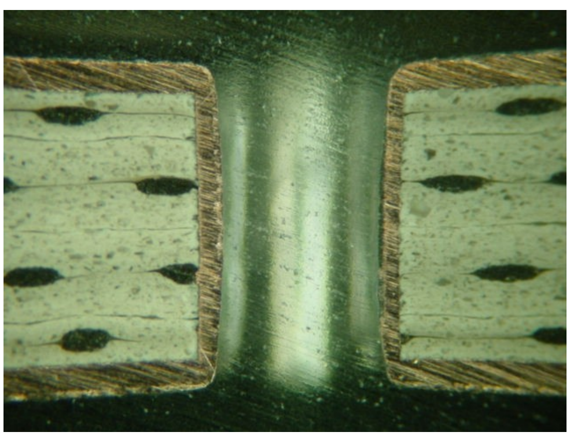

Figure 3 – Double Sized TacLam Hole Wall Quality

Taconic recommends the following drill conditions for TLG material:

- Entry material: Aluminum sheet or standard phenolic entry (10-15 mil Phenolic preferred)
- Backup material: Hard phenolic of thickness from 0.060” to 0.125”
- Stack height should not exceed 2/3 the flute length of the smallest diameter drill being used.
- Drill parameters as found in the drill appendix. For microdrilling (<0.020” diameter) use the highest speed column parameters that equipment allows.
- Optimize drill parameters to reduce or eliminate birdnesting, burrs, and smearing
- Hit counts range from 500 hits to 1000 hits depending on drill size and board thickness.
- Peck drilling if necessary

All drilling debris must be removed prior to hole wall preparation such as plasma or sodium treatment. Thoroughly remove all debris in the holes with a high pressure air or water blast. If water is used, bake the laminate for 1 hour at 250^o F [120^{o}C] to remove moisture prior to through hole treatment.

Burring can occur if drilling conditions are not correct. If burring occurs, sanding is not recommended. Pumice scrubbing has been known to be effective, however Taconic does not recommend any process that may cause distortion of the laminate. The best solution to prevent burrs is by thoroughly understanding and implementing the optimum drilling process and parameters for your equipment.

Smearing is a condition where the PTFE resin has been heated to a point where it softens and is easily moved within the hole. It usually appears as a line between the copper foil and the plated copper. Assuming that sharp drill bits are being used, the solution is to reduce the speed (thus surface feet per minute) and infeed to prevent the heating up of the drill bit. Low chip loads are the key to success in drilling PTFE. If debris builds up on the bits (birdnesting) it is necessary to optimize the thickness of the phenolic entry material. Phenolic entry material is a hard material that will abrade PTFE off the surface of the bit. If the drill tool is contaminated with PTFE in the flutes, the drill debris will strike an inner layer and smear drill bit debris across the post. The phenolic entry material should be used as a sacrificial material to smear drill bit debris onto the phenolic so that the drill bit reaches the PTFE laminate core free of any debris. Dwell times between hits will allow the bit to cool before reentry. Protrusions may not be noticeable until after the electroless plating process, even if a high magnification microscope is used. See Section 6 for hole-wall preparation. Hole wall tear-out, or gouging, is another possible defect caused during the drilling process. Gouging is usually an indicator of either a dull drill or an excessively high chip load. Another factor that can influence gouging is the fiberglass weave style. A coarse glass is more prone to gouging than a medium or fine glass style. If gouging occurs, first check for worn drill bits before adjusting the drill parameters. If gouging persists, reduce the chip load. Care should be taken to keep drill bit temperatures to a minimum by keeping the surface feet per minute low while adjusting chip loads downward.

Due to the thickness of high-layer-count digital multilayer boards, peck drilling may be required for acceptable hole wall quality. The thermoplastic nature of the PTFE resin and the thickness of the board may result in the inability of the drill bit to clear debris which may result in smearing and burrs. Peck drilling with a full withdrawal of the drill bit after each peck will reduce heat buildup and debris accrual. A general rule of thumb for peck depth is 20 to 30 mils per peck and should be optimized at the board shop.

Drilling Multilayers Containing TPG Prepreg

The typical material combination for RF / Microwave and digital multilayers are TLG/TPG, RF-35A/TPG and TSM-30/TPG.

Tight process control and optimized parameters are essential to achieve required hole wall quality for thick multilayer (> 0.100") and back plane. High speed digital application has tight specification to ensure that press fit connectors are not damaged.

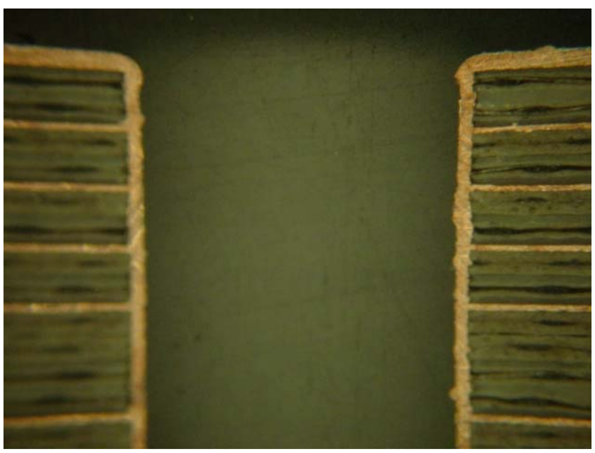

Figure 4 – Multilayer board made with TSM-30 and TacLam TPG-32

Drill setup conditions

(1) Drill bits: Use only new straight shank bits. For example:

a. Diameter < 15mil Tycom/Kyocera 560 series straight shank. A comparison of drill bit vendors yielded the following results for a 10 mil tool when drilling a 115 mil fastRise27/TSM multilayer stackup:

Vendor	Model	Helix Angle	Style	Nodules/hole
Union	NEU L026, 0.25x4.5	40	UC	0.54
Union	MD35 A3815, 0.25x5/#8	35	Straight	0.72
Kemmer	SH381010021021R	38	Straight	0.67
Kemmer	E34000250-C45040	38	UC	0.72
Kyocera/Tycom	460.0098.177	38	UC	0.98
Kyocera/Tycom	560.0098.177	38	Straight	0.12
HPTec	8 212 0250	40	UC	0.48
HPTec	212, 157mil flute	45	UC	0.25

Parameters: 10 mil Tycom 560 series straight shank, 7 mil aluminum entry, 16.5 mil phenolic entry, 16.5 mil phenolic exit, 120K speed, infeed 55, 0.25 second dwell between hits, 1st peck to the depth of phenolic + aluminum + 2 mils into material (28 mil), 1 peck/30 mils thereafter.

(2) Maximum hit counts: 200 hits/bit
(3) Drill Stackup Illustration (for 250 mil thick pwbs, thick phenolic entry should be used):

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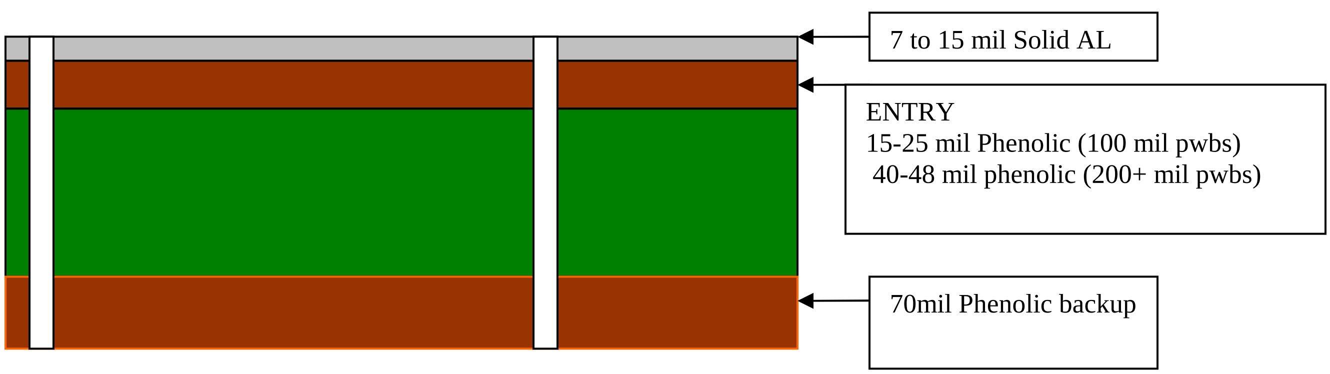

Figure 5 – Stackup of Multilayer Drilling

(4) Vacuum: Maximum capacity
(5) Drill foot pressure: > 40 psi
(6) Dwell between hits: 1 second (250 millisecond may work)
(7) Peck drilling through the phenolic entry material.

Table 4. Multilayer Drill Parameters

Drill Size (inch)	**Chipload** (mil)	**Spindle speed** (Krpm)	**Feed rate** (ipm)	**Retract Rate** (in/min)
0.010	0.4 -.6	80-125	55-60	1000
0.012	0.4 -.6	80-125	55-60	1000
0.0200	.64	70	45	1000
0.0280	1.0	32	32	1000
0.0380	1.3	24	31	1000
0.0400	1.8	22	40	1000
0.0420	1.8	21	38	1000
0.0440	1.8	20	37	1000
0.0460	1.8	19	35	1000
0.0480	1.8	19	34	1000
0.0500	2.0	18	36	1000

Table 4 – TacLam Multilayer Drill Parameters

Entry/Exit Materials

Phenolic entry and exit material is critical for drilling PTFE based circuit boards. 16-25 mil phenolic is recommended for 100 mil pwbs. 40-50 mil phenolic entry is recommended for 250 mil thick pwbs. PTFE gets hot and likes to accumulate on the surfaces of the bit. Phenolic entry and exit material will essentially “clean” the surface of a bit. Debris builds up on the bit which includes anything the bit comes into contact with: entry material, copper, fiberglass, silica, PTFE, metal from the bit itself, phenolic, Aluminum etc. It is necessary to use a hard thick phenolic entry material to essentially break the debris off the bit and smear the debris onto the phenolic before the bit arrives clean at the surface of the pcb and drills. Following these drill parameters should allow the user to arrive at fairly good hole wall quality on very thick telecom type boards (200-300 mil). DO NOT WORRY ABOUT PHENOLIC CAUSING EXCESSIVE DRILL WEAR. Drilling Teflon is limited by debris filling and fusing to the drill bits. Drill bits are exchanged due to debris build up on the bits before wear becomes an issue. Typically 70 mil phenolic is used as backup but the phenolic only needs to be 15 mils or the depth of the drill. If the drill only penetrates 20 mils at the bottom the phenolic need only be 20 mil. Phenolic backup can be stacked with spectrumboard. Phenolic can also be combined. A 25 mil piece of phenolic can be combined with a 15 mil piece of phenolic to yield a 40 mil piece of phenolic.

If the requirements are such that even higher hole wall quality is needed there is another solution:

Tip: Strategies to remove plating nodules: for very demanding hole wall specifications it might be necessary to drill the holes, pass the pcb through an electroless treatment or flash plating treatment to essentially make the debris in the hole rigid, then redrill to snap the debris from the side of the hole wall. Another strategy for critical hole wall quality is to slightly under drill (using undersized diameter drill bit?)the hole, thereby remove most of the PTFE-ceramic from the hole, flash plate the hole, and then redrill it with the proper size bit. If undersized drilling is used, flash plating between drill sizes may not be necessary.

Dwell Times

Studies have shown that the best hole wall quality is obtained when the drill bit has a chance to cool. This makes intuitive sense because a cooler bit will be less likely to cause the PTFE to become soft and stretchy. We have found that a 1 second (1,000 ms) dwell time between hits is sufficient. Longer dwell times will not improve hole wall quality.

Peck Drilling

We have also found that it is beneficial to “clean” the bit by pecking to a depth that corresponds to the thickness of the entry material. Pecking through the distance of the phenolic will abrade debris off the bit in the phenolic and allow the debris from the phenolic to be removed before the bit reenters the hole and starts drilling the multilayer based on TLG/TPG. Therefore the first peck should be the depth of the entry material. This is necessary to remove the phenolic debris before “cleaned” drill bit starts drilling into the PTFE based pcb. Past studies have shown that peck drilling inside of PTFE pcb is necessary for micro diameters (12mil and 14mil) to remove the debris in order to prevent tool breakage. However, for 28mil holes, peck drilling inside 200 mil PTFE based pcb is still not clear. Some drill studies suggest that peck drilling will leave a small circular ring where the drill bits stop in the hole. However, it may be necessary to peck drill to get the best overall hole wall quality.

Hole Wall Preparation

Due to the relative softness of PTFE resin, small fiberglass protrusions may occasionally occur. These protrusions will plate up and cause small nodules in the holes that may result in finished hole sizes being smaller than desired. If changes in drill parameters do not eliminate the fiber protrusions, it is recommended that the drilled hole size be increased to the maximum tolerance so that the finished hole size is within specification. Another method to reduce the size of the fiberglass protrusion is to use a glass etch process. Care should be taken to not overetch the glass as uneven hole walls or wicking into the fiber bundle may occur.

PTFE based laminates require that drilled holes be subjected to a process that will prepare the PTFE resin system for subsequent plating. Since TacLam® TLG contains

PTFE resin; it requires treatment prior to plating. There are two hole wall treatment processes that have been shown capable of providing void-free copper plating. One process is chemical in nature and involves a sodium-based solution that strips the fluorine atoms from the PTFE molecules. This process has been used for many years in the industry with great success. The advantages of sodium etching include long shelf life of the hole wall treatment, fast treatment time, and complete coverage. The primary disadvantage of sodium etchant is the volatility of the chemical. Various manufacturers and etchant services are available.

Another method of preparing the holes for plating is plasma etching. If the proper gases and cycles are used, plasma will allow plating to the PTFE resin. Experience has shown that the best gases to use are a mixture of hydrogen and nitrogen. Helium can also be used in many cases. The advantage of plasma etching is that it is a relatively safe procedure. Disadvantages include relatively long cycle times (35 to 60 minutes) and short shelf life of the effect (4 – 24 hours).

The TacLam® TLG product also contains a thermoset resin as the bonding agent. This requires a desmear process in addition to the PTFE treatment. There are also two common methods of desmearing thermoset resin systems. One of the desmear processes involves dipping the boards in a permanganate chemical which dissolves the resin. The second method is plasma. Generally speaking, the gases used to desmear the thermoset resin do not affect the PTFE resin, nor do the gases used for treating the PTFE resin desmear the thermoset resin very well if at all. Also, the sodium solution commonly used to treat the PTFE resin will not affect the thermoset resins system. No matter which method is used for desmearing the thermoset resin, the BT/epoxy resin should be desmeared prior to treatment of the PTFE resin.

Permanganate desmear has been shown to be very aggressive, due to the relatively small amount of BT/epoxy in the product, and can cause excessive etchback. Permanganate will not affect the PTFE resin found in TacLam. Desmearing of the BT epoxy can be more closely controlled with a plasma desmear cycle. In addition, hole wall treatment of the PTFE can also be done successfully with plasma and it is possible to have back-to-back desmear and hole treatment without removing the product from the plasma machine.

Taconic recommends the following hole wall treatment:

- Thoroughly clean holes prior to treatment. If water cleaning is used, bake the boards at 220^{o}F (105^{o}C) for 1 hour
- Plasma treat the epoxy component using a standard epoxy desmear gases and power and a 15 minute cycle time to reduce overetching of the epoxy

- Continue plasma cycle with a PTFE cycle shown below

Sodium Treatment: A sodium-based chemical treatment process does an excellent job of preparing the PTFE through-hole surface prior to the plated through hole process. Follow the manufacturer's recommended treatment process. Bake for 1 hour at 250^o F [120^{o}C] prior to plating to remove moisture that may have been absorbed during the sodium treatment process. NOTE: Do not subject the treated holes to heavily concentrated chlorine-based chemical processes prior to electroless copper plating or direct metallization. Chlorine can have adverse effects on the sodium treatment and result in plating voids.

Plasma Etching: Plasma treatment of the PTFE resin using a 30-70% Hydrogen, 70-30% Nitrogen gas mixture has been shown to be very effective. If Hydrogen is not available, a 100% Helium should also suffice. Power setting for the RF-signal generator should be 60-75% of full rated power for 30-60 minutes depending on the hole diameter, number of holes, and thickness of the board. Boards with relatively higher aspect ratios will require longer plasma cycle times. Industry experience has shown that gases such as helium and CF_4 are not as effective as hydrogen as evidenced by sporadic plating voids and higher contact angles.

Note: Regardless of which method of hole wall treatment is used, desmearing of the thermoset resin should be done prior to treatment of the PTFE resin.

Plating

After the hole wall has been properly prepared, TacLam® TLG will accept either electroless copper or direct metallization plating. The electrolytic plating process is the same for PTFE or epoxy based materials. Typical plating consists of 1 – 1.5 mils [25µm - 35µm] of copper plate in the holes and/or on the surface.

Image, Develop, Etch, Strip

Prepare the copper surface, apply dry film, and image and develop using a standard process. The copper surface preparation should consist of microetching the copper. Scrubbing is not recommended for thin core PTFE-based materials or multilayer inner layers due to possible registration issues.

The etching process is the same as for a standard printed circuit board. Machine settings should be appropriate for the copper thickness of the multilayer inner layers. Strip the photoresist using a standard process.

Solder Mask

TacLam® TLG readily accepts LPI solder mask and requires no special treatment.

Solder Reflow

Hot air solder leveling is a common method of protecting exposed copper circuitry. Two basic types of hot air level machines are used in the industry, horizontal and vertical. By far the more popular of the two is the vertical machine. It is less expensive and easier to maintain than the horizontal type. However, the vertical machine subjects the printed circuit board to a more severe level of thermal shock than the horizontal. Once the board is clamped in the vertical machine, the only preheat the board sees is the few seconds above the solder pot prior to immersion. Typical immersion times are 5 – 6 seconds from entry into the solder pot to complete withdrawal. This minimal preheat time can be particularly harsh on PTFE based laminates due to their z axis expansion characteristics. When using hot air solder leveling on PTFE laminates, Taconic recommends a bake cycle of 2 – 3 hours at 300^{o} F [150^{o}C] just prior to the HASL process. The solder pot temperature should be maintained at 460^{o} – 480^{o} F [238^{o}C – 250^{o}C] for optimal performance. Cycle time should be 5 – 6 seconds from the time of entry to the complete withdrawal of the board. Dwell time in the solder pot should not exceed 2 seconds.

Machining

Machining of TacLam® TLG is typically more difficult than epoxy-based substrates due to the softness of the PTFE resin system. The style of fiberglass used in the substrate also affects the quality of routing with respect to burrs and fibers. The heavier the fiberglass weave, the more difficult it is to cut.

TacLam® can be successfully machined using standard router bits or end mills when the recommended methods and rout parameters are used. In addition to the rout parameters, an equally important factor in successful routing is having intimate contact throughout the routed package. The following illustration shows a typical rout stack with phenolic entry and backer material on either side of the circuit board. Notice that the entry material rides on top of the copper traces leaving an air gap between the entry material and the PTFE substrate. Many circuit board applications also have soldermask on top of the copper traces which increases the gap further. The solution to a cleaner cut is to introduce a material between the copper traces and the phenolic entry material that will conform at the edge and will help fill in the air gap. As the router pressure foot applies pressure, the edge of the phenolic entry and the paper will conform and help fill the air gap, allowing for a cleaner cut of the substrate edge. One type of paper that has been shown to work well is the paper found between artwork film. It is thick and will conform enough to help fill in the normal air gap and cuts without generating as much debris as other paper such as Kraft paper.

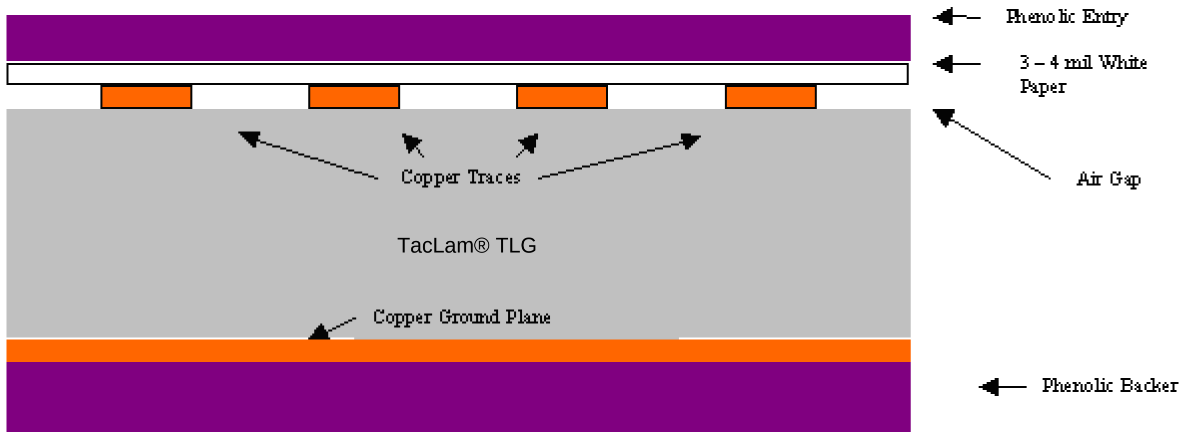

Figure 6 – Typical rout stack

The following routing parameters in Tables 4 and 5 have been proven to work well on PTFE double-sided boards and are good starting points for TacLam® multilayer boards with thicknesses of 0.060” [1.58mm] or less. For thicker multilayers, a single flute, 3/32” [2.38mm] carbide bit or a diamond burr tool has been shown to work well at an infeed rate of 24” [0.6m] per minute and a speed of 45,000 rpm.

Recommended Routing Parameters for All Taconic Materials							
		Spindle Type				**Z – Feed Rate**	
		60,000 max		**80,000 max**			
Tool Diameter (mils)	**Chipload** (mils/rev)	**Spindle Speed** (rpm)	**Feed Rate** (in/min)	**Spindle Speed** (rpm)	**Feed Rate** (in/min)	**Without predrilling** (in/min)	**With predrilling** (in/min)
31.5	0.24	50000	11.8	50000	11.8	0.0	20
35.4	0.26	45000	11.8	45000	11.8	0.0	20
39.4	0.30	40000	11.8	40000	11.8	0.0	79
43.3	0.32	37000	11.8	37000	11.8	0.0	79
47.2	0.35	34000	11.8	34000	11.8	0.0	79
51.2	0.51	31000	15.8	31000	15.8	0.0	79
55.1	0.54	29000	15.8	29000	15.8	0.0	79
59.1	0.59	27000	15.8	27000	15.8	0.0	79
63	0.79	25000	19.7	25000	19.7	0.0	197
66.9	0.82	24000	19.7	24000	19.7	0.0	197
70.8	1.03	23000	23.6	23000	23.6	0.0	197
74.8	1.12	21000	23.6	21000	23.6	0.0	197
78.7	1.38	20000	27.6	20000	27.6	0.0	197
82.7	1.58	20000	31.5	20000	31.5	0.0	197
86.6	1.58	20000	31.5	20000	31.5	0.0	197
90.6	1.58	20000	31.5	20000	31.5	0.0	197
94.5	1.77	20000	35.4	20000	35.4	0.0	197
98.4	1.77	20000	35.4	20000	35.4	0.0	197
118.1	2.17	20000	43.3	20000	43.3	0.0	197
125	2.17	20000	43.3	20000	43.3	0.0	197

Table 5 – Recommended routing parameters for all Taconic materials

Suggested Routing Parameters for All Taconic Materials (metric)							
		Spindle Type				Z – Feed Rate	
		60,000 max		80,000 max			
Tool Diameter (mm)	**Chipload** (µm/rev)	**Spindle Speed** (rpm)	**Feed Rate** (m/min)	**Spindle Speed** (rpm)	**Feed Rate** (m/min)	**Without predrilling** (m/min)	**With predrilling** (m/min)
0.80	5	50000	0.25	50000	0.25	0	0.50
0.90	6	45000	0.27	45000	0.27	0	0.50
1.00	8	40000	0.32	40000	0.32	0	2.00
1.10	9	37000	0.33	37000	0.33	0	2.00
1.20	10	34000	0.34	34000	0.34	0	2.00
1.30	12	31000	0.37	31000	0.37	0	2.00
1.40	14	29000	0.41	29000	0.41	0	2.00
1.50	16	27000	0.43	27000	0.43	0	2.00
1.60	18	25000	0.45	25000	0.45	0	5.00
1.70	22	24000	0.53	24000	0.53	0	5.00
1.80	26	23000	0.60	23000	0.60	0	5.00
1.90	30	21000	0.63	21000	0.63	0	5.00
2.00	34	20000	0.68	20000	0.68	0	5.00
2.10	38	20000	0.76	20000	0.76	0	5.00
2.20	40	20000	0.80	20000	0.80	0	5.00
2.30	42	20000	0.84	20000	0.84	0	5.00
2.40	44	20000	0.88	20000	0.88	0	5.00
2.50	46	20000	0.92	20000	0.92	0	5.00
3.00	53	20000	1.06	20000	1.06	0	5.00
3.18	55	20000	1.10	20000	1.10	0	5.00

Table 6 – Recommended routing parameters for all Taconic materials (metric)

Appendix

TacLam® TLG Microdrilling Parameters								
		80,000 max		110,000 max		125,000 max		
Drill Size	Chipload	Spindle Speed	Feed Rate	Spindle Speed	Feed rate	Spindle Speed	Feed Rate	Retract Rate
(in)	(mil)	(rpm)	(in/min)	(rpm)	(in/min)	(rpm)	(in/min)	(in/min)
0.0039	0.3	80,000	24	110,000	35	125,000	39	118
0.0059	0.5	80,000	39	110,000	55	125,000	63	177
0.0079	0.7	80,000	59	110,000	79	125,000	91	236
0.0098	1.0	80,000	79	110,000	106	125,000	122	295
0.0118	1.2	80,000	94	110,000	130	125,000	146	354
0.0138	1.3	80,000	106	110,000	146	119,000	157	413
0.0157	1.5	80,000	118	104,000	154	104,000	154	472
0.0177	1.7	80,000	134	92,000	154	92,000	154	531
0.0197	1.9	80,000	150	83,000	157	83,000	157	590

Table 7 – TacLam® TLG microdrilling parameters

TacLam® TLG Drilling Parameters									
Drill Size	Chipload	Spindle speed	Feed rate	Retract Rate	Drill Size	Chipload	Spindle speed	Feed rate	Retract Rate
(in)	(mil)	(rpm)	(in/min)	(in/min)	(in)	(mil)	(rpm)	(in/min)	(in/min)
0.0217	1.8	80,000	140	400.0	0.0748	2.4	27,000	65	500.0
0.0236	1.8	77,500	141	400.0	0.0768	2.5	26,000	65	500.0
0.0256	1.9	75,000	140	400.0	0.0787	2.5	26,000	65	500.0
0.0276	1.9	72,500	135	400.0	0.0807	2.5	26,000	65	500.0
0.0295	1.9	70,000	130	400.0	0.0827	2.6	25,000	65	500.0
0.0315	1.9	66,000	125	400.0	0.0846	2.7	24,000	65	500.0
0.0335	1.9	62,000	120	400.0	0.0866	2.7	24,000	65	500.0
0.0354	2.0	60,000	120	500.0	0.0886	2.8	23,000	65	500.0
0.0374	2.0	57,000	115	500.0	0.0906	2.8	23,000	65	500.0
0.0394	2.0	54,000	110	500.0	0.0925	2.7	22,000	60	500.0
0.0413	2.1	51,000	105	500.0	0.0945	2.8	21,500	60	500.0
0.0433	2.1	48,000	100	500.0	0.0965	2.6	21,000	55	500.0
0.0453	2.1	45,000	95	500.0	0.0984	2.7	20,500	55	500.0
0.0472	2.1	43,000	90	500.0	0.1004	2.5	20,000	50	500.0
0.0492	2.0	42,000	85	500.0	0.1024	2.5	20,000	50	500.0
0.0512	2.0	40,000	80	500.0	0.1043	2.5	20,000	50	500.0
0.0531	2.1	39,000	80	500.0	0.1063	2.3	19,500	45	500.0
0.0551	2.1	38,000	80	500.0	0.1083	2.3	19,500	45	500.0
0.0571	2.2	36,000	80	500.0	0.1102	2.4	19,000	45	500.0
0.0591	2.4	34,000	80	500.0	0.1122	2.2	18,500	40	500.0
0.0610	2.3	32,000	75	500.0	0.1142	2.2	18,500	40	500.0
0.0630	2.3	32,000	75	500.0	0.1161	2.2	18,000	40	500.0
0.0650	2.3	32,000	75	500.0	0.1181	2.0	17,500	35	500.0
0.0669	2.4	31,000	75	500.0	0.1201	2.0	17,500	35	500.0
0.0689	2.3	30,000	70	500.0	0.1220	2.1	17,000	35	500.0
0.0709	2.4	29,000	70	500.0	0.1240	1.8	17,000	30	500.0
0.0728	2.5	28,000	70	500.0	0.1250	1.9	16,000	30	500.0

Table 8 – TacLam® TLG drilling parameters

TacLam® TLG Microdrilling Parameters (Metric)								
		80,000 max		110,000 max		125,000 max		
Drill Size (mm)	Chipload (um)	Spindle Speed (rpm)	Feed Rate (m/min)	Spindle Speed (rpm)	Feed Rate (m/min)	Spindle Speed (rpm)	Feed Rate (m/min)	Retract Rate (m/min)
0.10	7.6	80,000	0.61	110,000	0.89	125,000	1.00	2.99
0.15	12.5	80,000	1.00	110,000	1.40	125,000	1.60	4.49
0.20	18.8	80,000	1.50	110,000	2.00	125,000	2.30	5.98
0.25	25.0	80,000	2.00	110,000	2.70	125,000	3.10	7.48
0.30	30.0	80,000	2.40	110,000	3.30	125,000	3.70	8.98
0.35	33.7	80,000	2.70	110,000	3.70	119,000	4.00	10.47
0.40	37.5	80,000	3.00	104,000	3.90	104,000	3.90	11.97
0.45	42.5	80,000	3.40	92,000	3.90	92,000	3.90	13.47
0.50	47.5	80,000	3.80	83,000	4.00	83,000	4.00	14.96

Table 9 – TacLam® TLG microdrilling parameters (metric)

TacLam® TLG Drilling Parameters (Metric)								
Drill Size (mm)	Chipload (um)	Spindle speed (rpm)	Feed Rate (m/min)	Retract Rate (m/min)	Drill Size (mm)	Chipload (um)	Spindle Speed (rpm)	Feed Rate (m/min)
0.55	44.4	80,000	3.55	10.2	1.90	61.1	27,000	1.65
0.60	46.2	77,500	3.58	10.2	1.95	63.5	26,000	1.65
0.65	47.4	75,000	3.55	10.2	2.00	63.5	26,000	1.65
0.70	47.3	72,500	3.43	10.2	2.05	63.5	26,000	1.65
0.75	47.1	70,000	3.30	10.2	2.10	66.0	25,000	1.65
0.80	48.1	66,000	3.17	10.2	2.15	68.7	24,000	1.65
0.85	49.1	62,000	3.05	10.2	2.20	68.7	24,000	1.65
0.90	50.8	60,000	3.05	12.7	2.25	71.7	23,000	1.65
0.95	51.2	57,000	2.92	12.7	2.30	71.7	23,000	1.65
1.00	51.7	54,000	2.79	12.7	2.35	69.2	22,000	1.52
1.05	52.3	51,000	2.66	12.7	2.40	70.8	21,500	1.52
1.10	52.9	48,000	2.54	12.7	2.45	66.5	21,000	1.40
1.15	53.6	45,000	2.41	12.7	2.50	68.1	20,500	1.40
1.20	53.1	43,000	2.28	12.7	2.55	63.5	20,000	1.27
1.25	51.4	42,000	2.16	12.7	2.60	63.5	20,000	1.27
1.30	50.8	40,000	2.03	12.7	2.65	63.5	20,000	1.27
1.35	52.1	39,000	2.03	12.7	2.70	58.6	19,500	1.14
1.40	53.4	38,000	2.03	12.7	2.75	58.6	19,500	1.14
1.45	56.4	36,000	2.03	12.7	2.80	60.1	19,000	1.14
1.50	59.7	34,000	2.03	12.7	2.85	54.9	18,500	1.02
1.55	59.5	32,000	1.90	12.7	2.90	54.9	18,500	1.02
1.60	59.5	32,000	1.90	12.7	2.95	56.4	18,000	1.02
1.65	59.5	32,000	1.90	12.7	3.00	50.8	17,500	0.89
1.70	61.4	31,000	1.90	12.7	3.05	50.8	17,500	0.89
1.75	59.2	30,000	1.78	12.7	3.10	52.3	17,000	0.89
1.80	61.3	29,000	1.78	12.7	3.15	44.8	17,000	0.76
1.85	63.5	28,000	1.78	12.7	3.18	47.6	16,000	0.76

Table 10 – TacLam® TLG drilling parameters (metric)